

FIG. 1

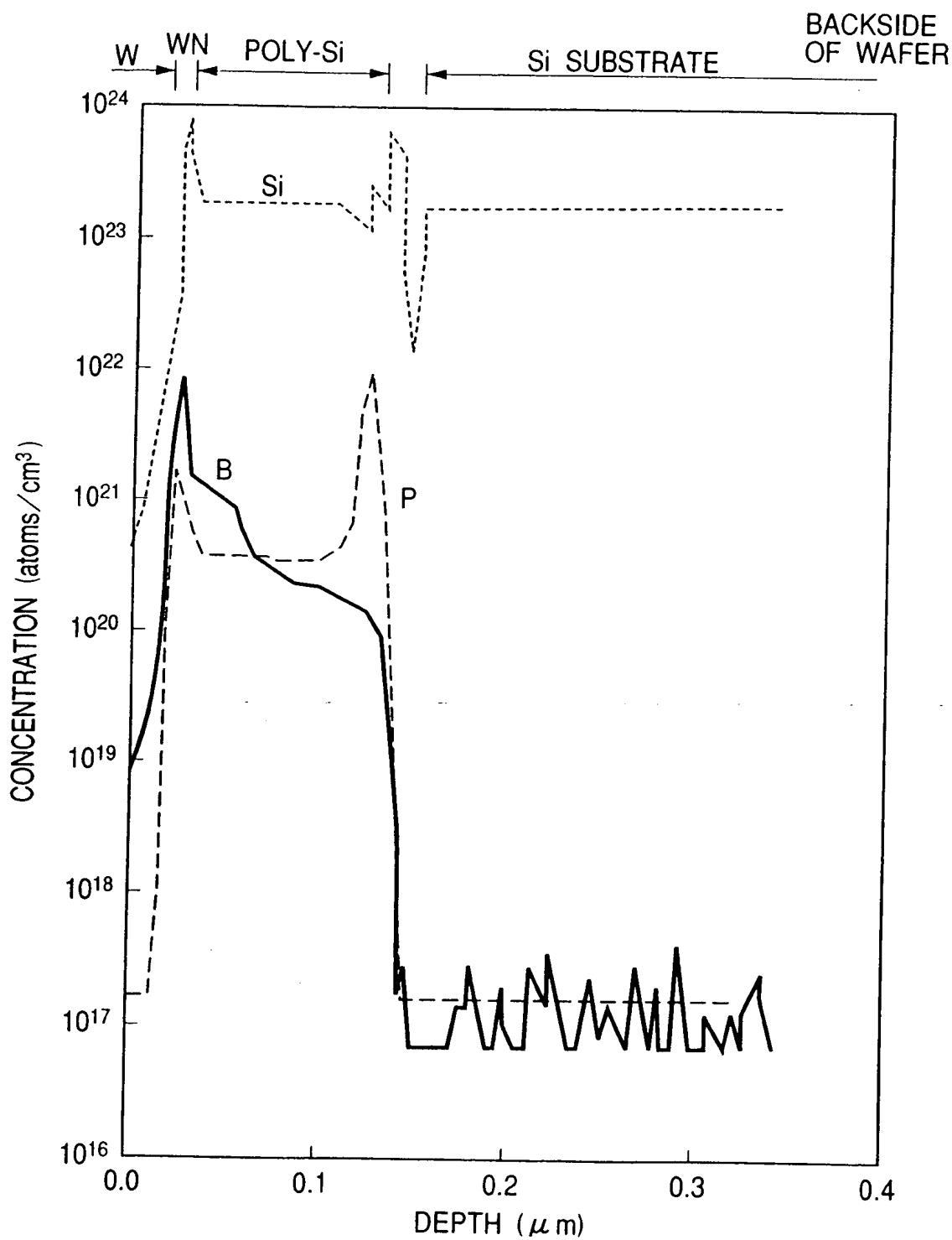
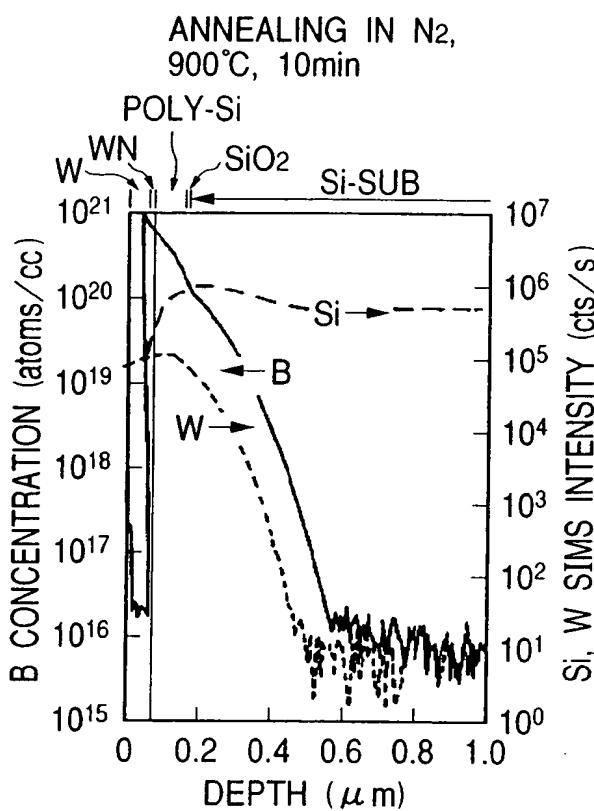
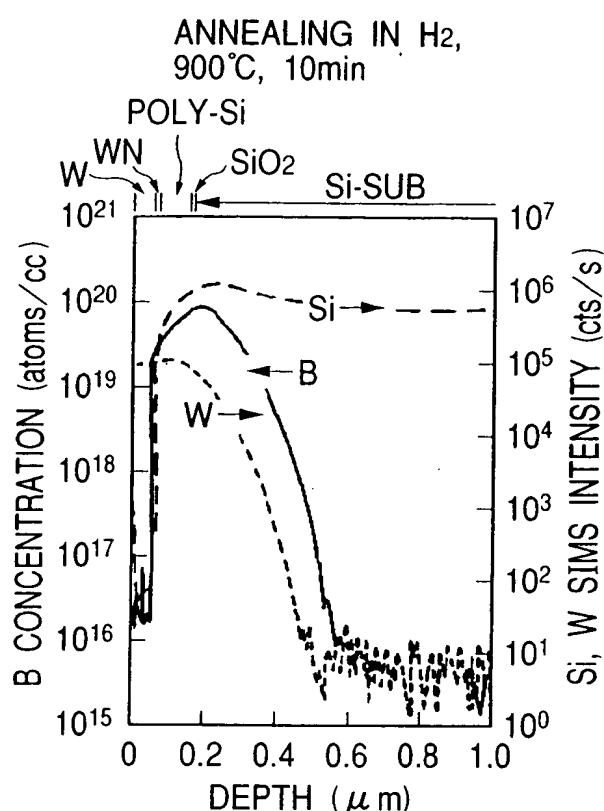


FIG. 2A**FIG. 2B****FIG. 2C**

ANNEALING IN H₂
WITH 5%H₂O,
900°C, 10min

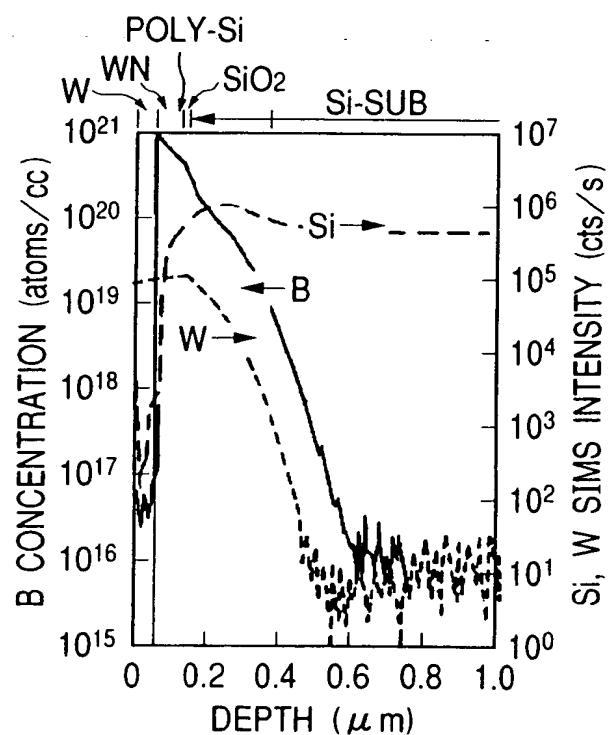


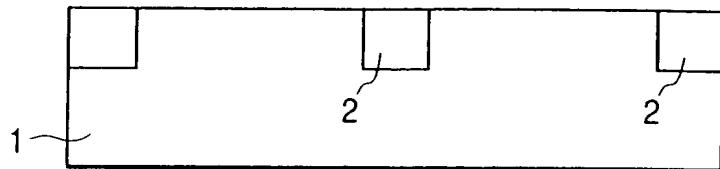
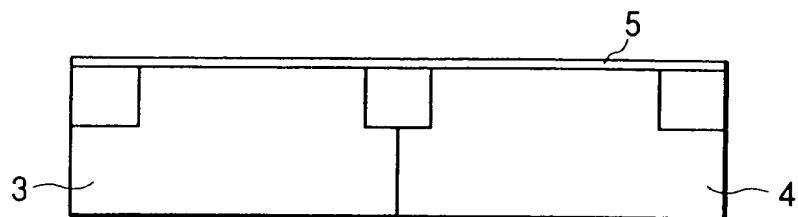
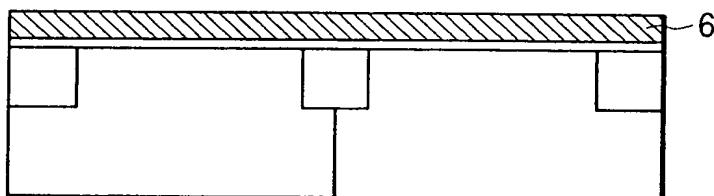
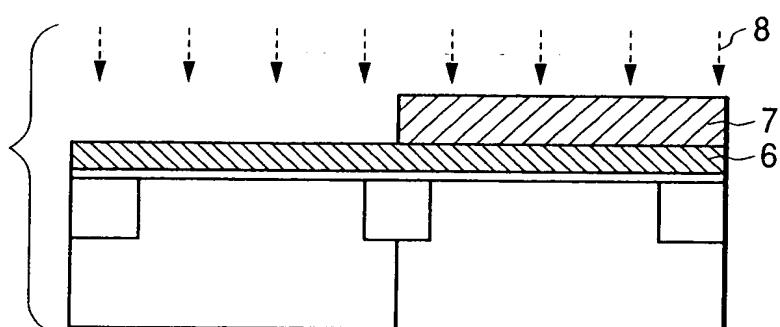
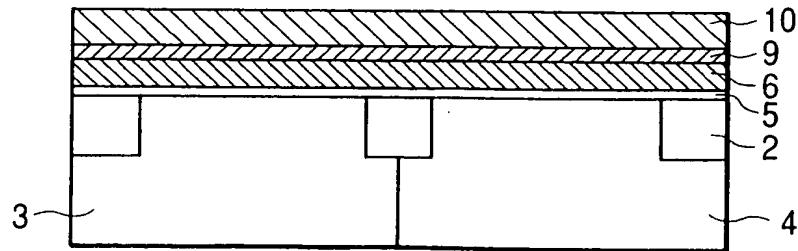
FIG. 3A**FIG. 3B****FIG. 3C****FIG. 3D****FIG. 3E**

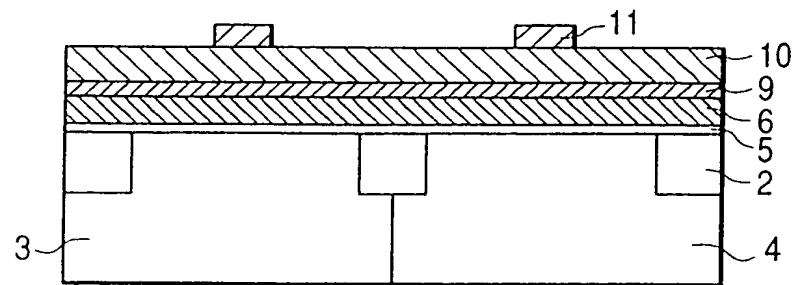
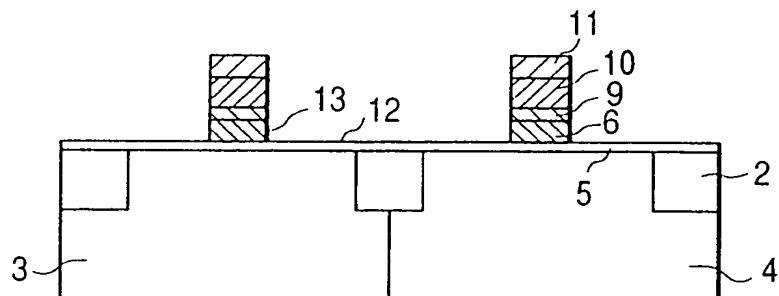
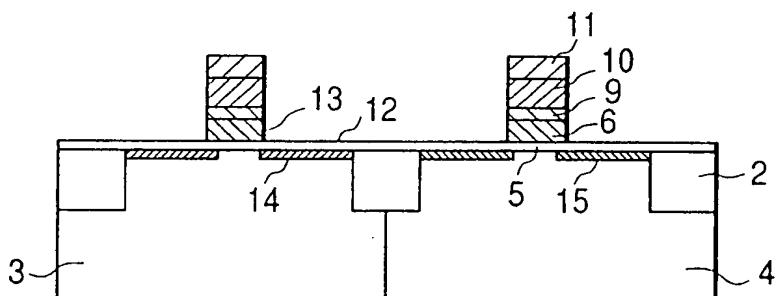
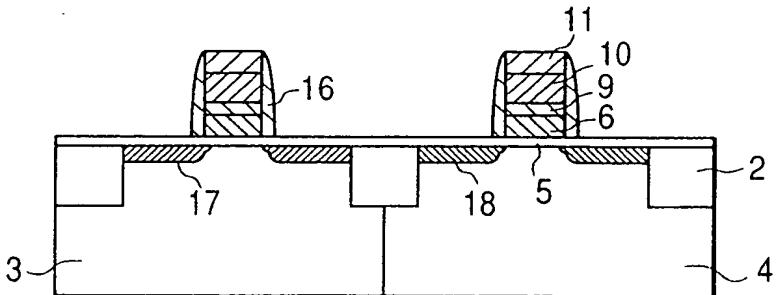
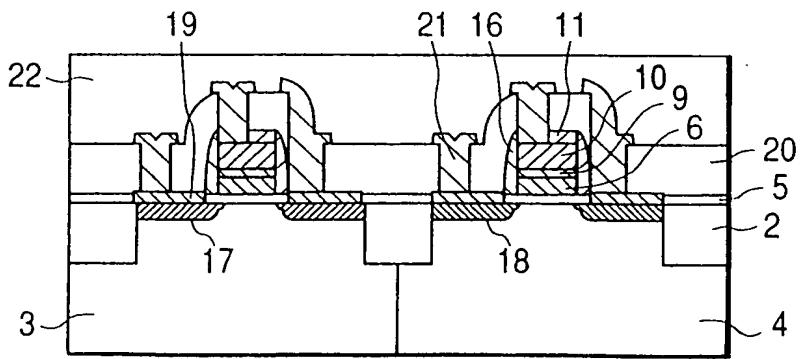
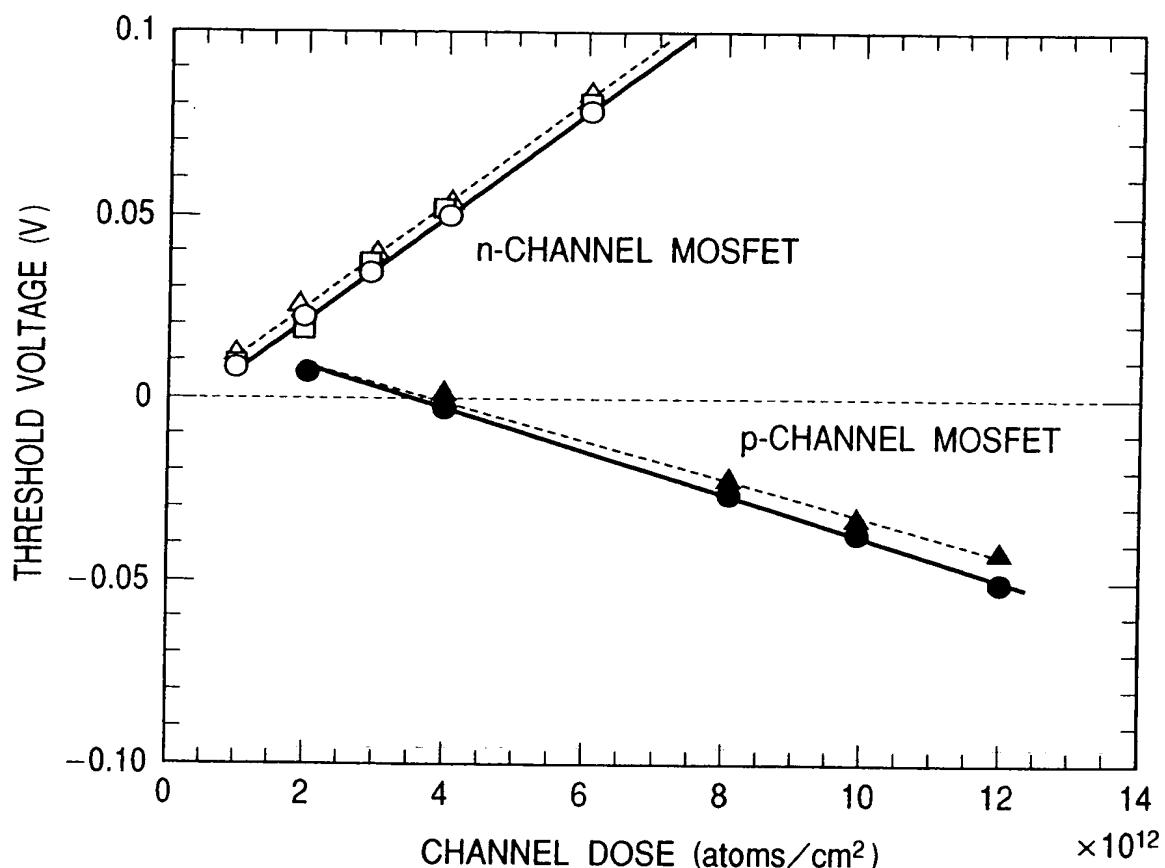
FIG. 4A*FIG. 4B**FIG. 4C**FIG. 4D**FIG. 4E*

FIG. 5



W/WN/POLY-Si GATE
(THIS WORK) { ● p-CHANNEL MOSFET
○ n-CHANNEL MOSFET

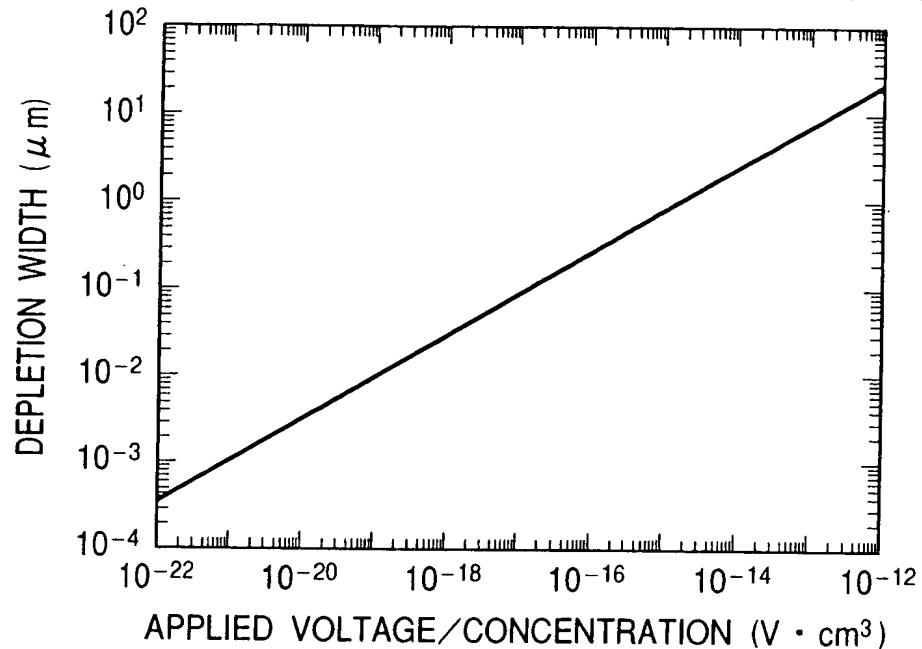
W/WN/POLY-Si GATE
(PREVIOUS) { ▲ p-CHANNEL MOSFET
△ n-CHANNEL MOSFET

POLY-Si GATE
(CONVENTIONAL)

□ n-CHANNEL MOSFET

FIG. 6A

RELATIONSHIP BETWEEN DEPLETION WIDTH AND
APPLIED VOLTAGE/CONCENTRATION OF SUBSTRATE

***FIG. 6B***

RELATIONSHIP BETWEEN BREAKDOWN VOLTAGE OF
pn JUNCTION AND CONCENTRATION OF SUBSTRATE

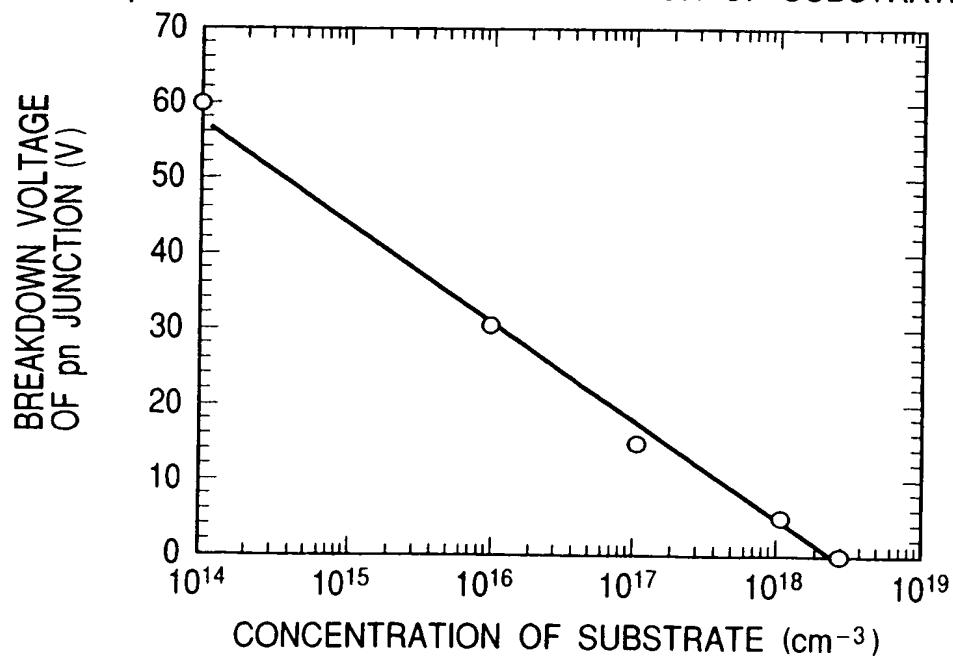


FIG. 7

